Hi3560Q Network Media Processor

Main Features

CPU Core
- ARM926EJ-S, 16-KB instruction cache and 16-KB data cache
- Built-in 2 KB instruction tightly-coupled memory
- 32-bit RISC processor in the Harvard architecture
- DSP enhanced architecture with 32 x 16 MAC
- Java hardware acceleration
- Built-in MMU to support multiple open operating systems
- Up to 270 MHz operating frequency

Video Decoding
- H.264 MP @ Level 3.0
- MPEG-1 (ISO/IEC 11172-2)
- MPEG-2 (ISO/IEC 13818-2) MP @ ML
- MPEG-4 ASP @ Level 5.0 or earlier and SP @ Level 3.0 or earlier
- DivX 4/5/6
- Xvid
- JPEG decoding, supporting up to 16 megapixel quick decoding.

Graphics Processing
- Video and image horizontal/vertical scaling
- Five overlapped hardware graphic layers support various graphic data formats
- Video denoising and image enhancement
- Three-field de-interlace and two-field interleave de-interlace processing with motion detection, median filter, and edge detection
- Anti-flick processing
- Supporting the RGB dithering
- Gamma correction
- Two-dimensional graphic acceleration engine, supporting games and abundant graphic interfaces

Audio Processing
- Processing various types of audio effects through the ARM core
  - MPEG1 L1/2/3, 2 channels, 16 bits, sampling rate 32/44.1/48 kHz
  - MPEG2 L1/2/3, 2 channels, 16 bits, sampling rate 32/44.1/48 kHz
  - MPEG2 AAC decoding, 2 channels, 16 bits, sampling rate 32/44.1/48 kHz
  - MPEG4 AAC LC/HE decoding, 2 channels, 16 bits, sampling rate 32/44.1/48 kHz
  - AC3 ByPass/Down Mix

Encryption Engine
- Implementing various encryption and decryption algorithms such as AES, DES, and 3DES through the hardware
- Being compatible with various CA solutions and supporting DVB descrambling
- Supporting the Macrovision 7.1 copy protection (optional)

Video Interfaces
- Integrated TV encoding in PAL or NTSC standard
- Integrated four-channel video DAC, supporting the YPbPr/RGB, CVBS, and S-Video output formats

Audio Interfaces
- One I^2S audio interface with an input channel and an output channel
- 16-/24-/32-bit sampling accuracy supported by the I^2S interface, with configurable sampling rate
- PCM interface
- SPDIF audio output interface

Ethernet Interfaces
- MII interface with the transmission speed of 10/100 Mbit/s
- MDIO interface

Transport Stream Interfaces
- Supporting transport stream input interface
- ISO 13818-1 MPEG-2 transport stream, supporting serial/parallel interface
- 32 PID filtering

Peripheral Interfaces
- Smart card interface, supporting the ISO/IEC 7816 protocol and the EMV standard
- USB 2.0 OTG interface, supporting low-speed, full-speed, and high-speed rates
- UART and I^2C interface
- IR interface
- GPIO and keyboard interfaces

External Memory Interfaces
- Supporting the DDR SDRAM interface with 16-bit data width
- Supporting the external expansion bus interface with 8-/16-bit data width, connecting to the external SRAM, ROM, and NORFlash

Network Protocols
- Supporting TCP/IP stack

Embedded Operating System
- Supporting Linux, WinCE, and VxWorks

Physical Specifications
- Typical power consumption: 1.0 W
- Multiple-level power-saving modes
- Technology: 0.13 μm
- Chip supply voltage: 1.2/2.5/3.3 V
- Operating temperature: 0–70℃
- Package: QFP256
- Dimension: 28 mm x 28 mm x 3.23 mm
- Pin pitch: 0.4 mm

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Chip Introduction

The Hi3560Q is a network media processor based on the ARM9 processor core and the hard acceleration engine. It is highly integrated and programmable, and supports multiple video and audio protocols. In addition to the efficient video and graphics processing units, the Hi3560Q also provides multiple reliable security solutions. It can be applied to various multi-media terminals, such as digital video broadcasting (DVB) bidirectional television set-top box (STB) and DVB/Internet Protocol (IP) dual-mode digital television STB.

The video processing unit supports real-time decoding that complies with various protocols, such as H.264, MEPG-1, MPEG-2, MPEG-4, Xvid, and Dvix. The advanced video compression technology makes it possible to provide video programs of large capacities through limited bandwidth. Moreover, multiple video decoding protocols are supported; therefore, more video sources are available.

The graphics processing unit provides the following functions:

- Video denoising and the image enhancement
- Video and image scaling and de-interlace processing
- On-screen display (OSD) and two-dimensional image acceleration

The preceding functions assist in developing the application graphic interface.

In addition, the Hi3560Q provides varied reliable security solutions.

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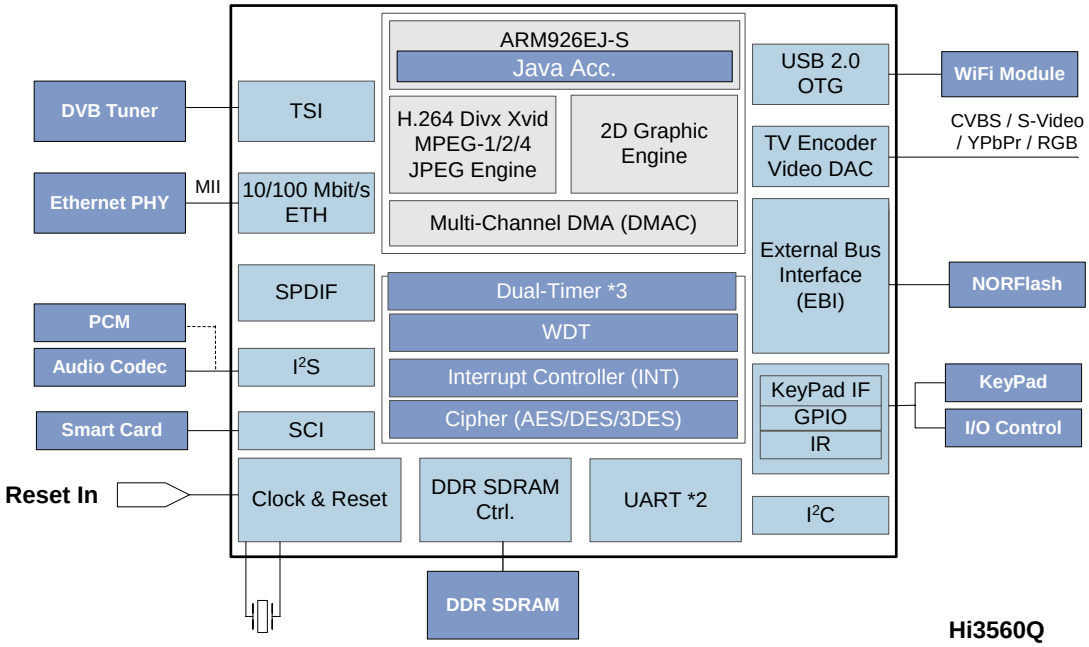
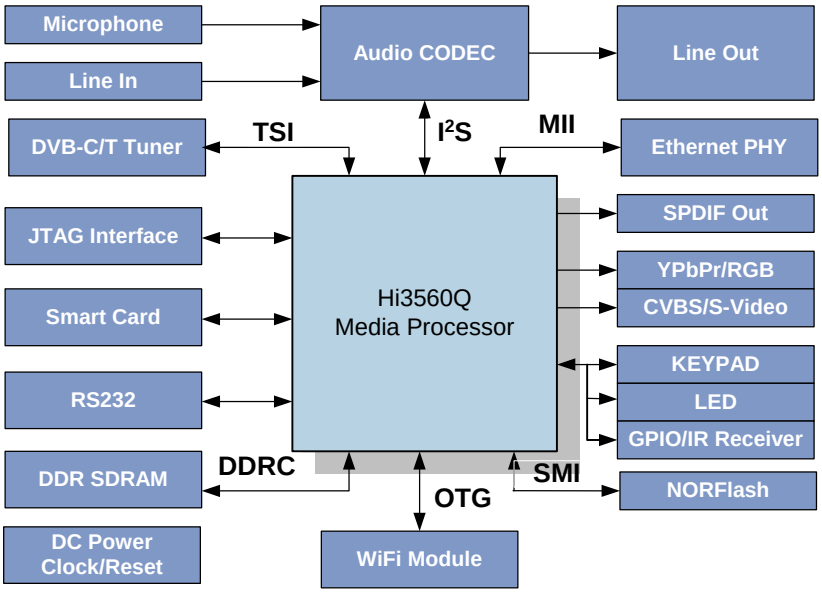
Block Diagram of Chip Functions



Application Field

- DVB bidirectional digital television STB
- DVB/IP dual-mode digital television STB

System Block Diagram of the Typical Hi3560Q Application



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